Paper Awards

Congratulations to the DesignCon Paper Award Winners!

DesignCon Paper Awards recognize contributions to the educational goals of the DesignCon program. Papers are judged both on the merits of the written document and on the quality of their presentation at DesignCon 2009.

Chip-Level Design Category:

1-WA2 | Design Space Exploration for High Performance Signal Processing Hardware using ESL Design Methodologies

Nitin Chawla, Senior Member of Technical Staff, STMicrolelctronics PvT
Pierre Busson, Advanced Architect Expert, STMicrolelctronics PvT
Thierry Michel, HW Staff Engineer, STMicrolelctronics PvT
Gagan Midha, Senior Design Engineer, STMicrolelctronics PvT
Harvinder Singh, Technical Specialist, STMicrolelctronics PvT
Pascal Urard, Director System Methods, STMicrolelctronics PvT

3-TA4 | Toward Harnessing the True Potential of IP Reuse

Kathryn Kranen, Chief Executive Officer, Jasper Design Automation
Homayoon Akhiani, Principal Engineer, Jasper Design Automation
Yann Antonioli, Program Director, Jasper Design Automation
Craig Deaton, Principal Methodology Engineer, Jasper Design Automation
Norris Ip, Director, Engineering, Jasper Design Automation
Lawrence Loh, Director, Application Engineering, Jasper Design Automation
Rajeev Ranjan, Chief Technology Officer, Jasper Design Automation

Board and System Design Category:

4-WP1 | SSO Noise, Eye Margin, and Jitter Characterization for I/O Power Integrity

Vishram Pandit, Senior Analog Engineer, Intel
Myoung Choi, Design Engineer, Intel
Hsiao-ching Chuang, Intel
Ashish Pardiwala, Design Engineer, Intel
Ruhul Quddus, Intel

5-TP2 | A Simple Via Experiment

Michael Steinberger, Distinguished Member of Technical Staff, Signal Integrity Software
Stephen Scearce, High Speed Design Group Manager, Cisco Systems
Douglas White, High Speed Design Specialist, Cisco Systems

Interconnect Design Category:

7-TA2 | Practical Analysis of Backplane Vias for 5 Gbps and Above

Eric Bogatin, President, Bogatin Enterprises
Sanjeev Gupta, Signal Integrity Specialist, Agilent
Mike Resso, Signal Integrity Measurement Specialist, Component Test Division, Agilent
Bert Simonovich, Signal Integrity and Backplane Architecture, Nortel

7-TH2 | New Serial Link Simulation Process, 6 Gbps SAS Case Study

Donald Telian, SI Consultant
Ravinder Ajmani, Senior Engineer, Hitachi GST
Kent Dramstad, Applications Engineer, IBM
Adge Hawes, Development Architect, IBM
Paul Larson, Senior Engineer, Hitachi GST

High-Speed and RF Design Category:

9-WP2 | 40/100 Gbps Transmission Over Copper: Myths and Realities

Ali Enteshari, Ph.D. Candidate, Center for Information and Communications Technology Research, The Pennsylvania State University
Mohsen Kavehrad, Professor, The Pennsylvania State University

11-WP2 |EMI from Multi-Gigabit SerDes Differential Pairs

Philippe Sochoux, EMC Design Manager, Central Engineering, Cisco Systems
Alpesh Bhobe, EMC Design Engineer, Cisco Systems
Jinghan Yu, EMC Design Engineer, Cisco Systems
Morris Hsu, Intern, Cisco Systems Morris Hsu, Intern, Cisco Systems

Power Integrity and Power-Award Design Category:

10-WA3 | Examining the Impact of Split Planes on Signal and Power Integrity

Jason Miller, Senior Staff Engineer, Sun Microsystems
Gustavo Blando, Signal Integrity Staff Engineer, Sun Microsystems
Roger Dame, Senior Staff Engineer, Sun Microsystems
K. Barry A. Williams, Principal Engineer, Sun Microsystems
Istvan Novak, Distinguished Engineer, SPARC Volume Servers, Sun Microsystems

Test and Measurement Category:

12-WA1 | Measurement-Assisted Electromagnetic Extraction of Interconnect Parameters on Low-Cost FR-4 boards for 6-20 Gbps Applications

Yuriy Shlepnev, President, Simberian
Alfred Neves, Senior Staff Signal Integrity Engineer, Teraspeed Consulting Group
Tom Dagostino, Vice President Engineering, Teraspeed Labs
Scott McMorrow, President, Teraspeed Consulting

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